

A stackable cross point phase change memory

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Abstract

A novel scalable and stackable nonvolatile memory technology suitable for building fast and dense memory devices is discussed. The memory cell is built by layering a storage element and a selector. The storage element is a Phase Change Memory (PCM) cell [1] and the selector is an Ovonic Threshold Switch (OTS) [2]. The vertically integrated memory cell of one PCM and one OTS (PCMS) is embedded in a true cross point array. Arrays are stacked on top of CMOS circuits for decoding, sensing and logic functions. A RESET speed of 9 nsec and endurance of 10^6 cycles are achieved. One volt of dynamic range delineating SET vs. RESET is also demonstrated.

Introduction

PCM arrays with different selectors have been disclosed. In a 0T1R configuration [3], the small read and write windows pose a severe limitation to the size of the array. In a 1T1R configuration [4], the paired MOS selector limits the layout at $8\lambda^2$ or higher. Using a crystalline bipolar selector [5, 6], cell sizes could approach $\sim 5\lambda^2$; however, decoding and selecting CMOS circuits share the substrate with silicon selectors, resulting in reduced array efficiency. Recent advances in thin film diode technology improve layout efficiency and stack-ability [7] but the on-off ratio of the thin film selectors will limit the size of each array partition. In this work, a thin-film two-terminal Ovonic Threshold Switch is deployed as the selector of a memory cell. The symmetrical blocking or triggering voltage, a.k.a. the threshold voltage, of the amorphous alloy [8] provides the base for a robust inhibiting scheme to isolate individual PCM cells in the cross point array. OTS shares the matched physical and electrical properties for PCM scaling. Given the compatibility of thin-film PCMS with mainstream metallization schemes, multiple layers of cross point memory arrays are feasible. Also, this back-end technology is fully stackable over CMOS circuits to achieve excellent array-efficiency and reduced die size.

The Memory Cell

The physical construction of a memory cell is shown in Fig. 1. The vertical stack of a PCMS cell consists of a top electrode connecting to a column metal, an OTS and a PCM interlinked by a middle electrode, and a bottom electrode connecting to a row metal. The IV characteristics are shown in Fig. 2. SET and RESET states are delineated by the threshold voltages.

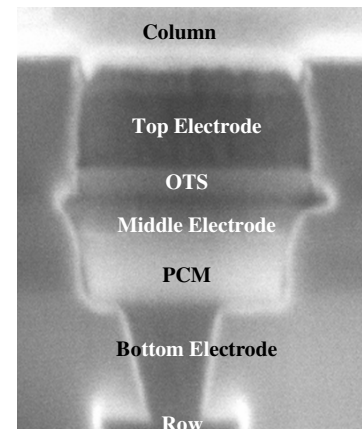


Fig. 1. SEM cross section of a PCMS cell.

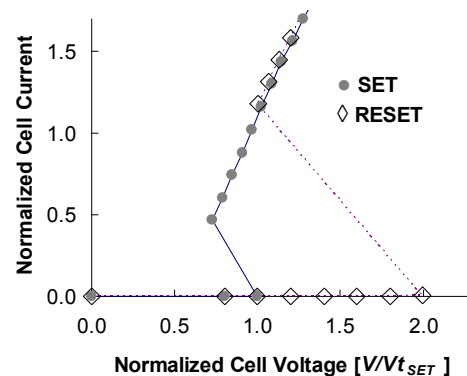


Fig. 2. The I-V Characteristics of a PCMS cell in SET and RESET. Voltage is normalized to the threshold voltage of the SET state, $V_{t\text{set}}$. Cell current is normalized to melting current, I_{melt} , the least current required to amorphize the material. (see Fig. 4)

The SET state exhibits lower threshold voltage than the RESET state. The threshold switching characteristics of OTS determine the threshold and sub-threshold of the SET state. The higher threshold voltage of the RESET state is attributed to the serial connection of two amorphous alloys, OTS and amorphous PCM. These IV characteristics shown in Fig. 3 are taken after a RESET pulse.

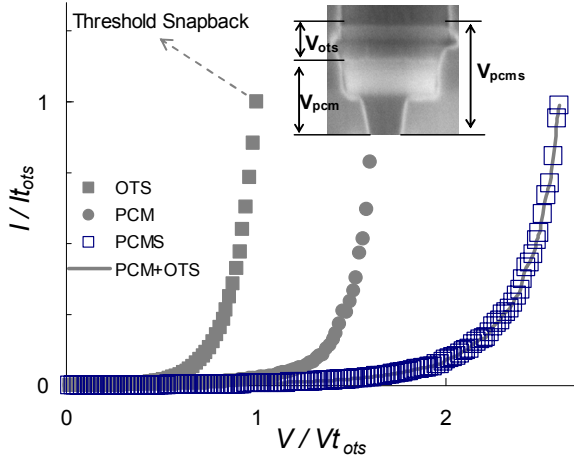


Fig. 3 PCMS = PCM + OTS; The threshold behavior of a RESET PCMS is equal to the additive result of the thresholds of OTS and amorphous PCM in series. Voltage and current are normalized to the threshold voltage and threshold current of OTS, $V_{t_{ots}}$ and $I_{t_{ots}}$ respectively.

The programming transfer characteristics are illustrated in Fig. 4. When current pulse amplitudes are lower than the melting current level, I_{melt} , PCM is crystallized to a SET-state (low resistance.) The SET-state threshold voltage, $V_{t_{set}}$, reflects OTS threshold switching characteristics. The higher threshold voltage at RESET state is attributed to the addition of amorphous PCM subject to electrical pulsing amplitude higher than I_{melt} .

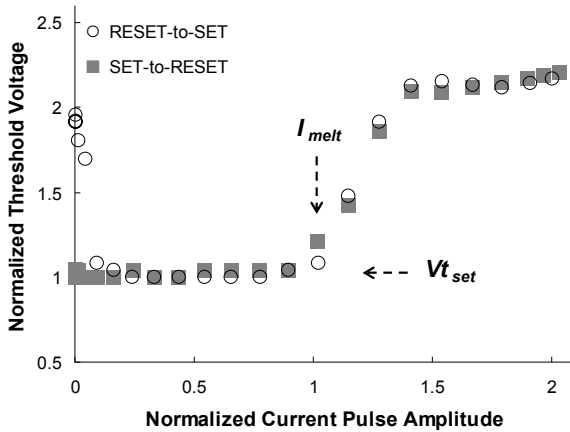


Fig. 4. Single cell PCMS electrical programming characteristics. Current and voltage are normalized to I_{melt} and $V_{t_{set}}$, respectively. Each point is conditioned to the same initial states correspondingly.

The Cross Point Array

With its low temperature processing, the thin-film PCMS is inherently compatible with the present state of backend metallization technologies. Therefore, the X/Y cross point array does not require additional strapping for low parasitic resistance. The strapless cross point topology provides an ideal scaling path for $4\lambda^2$ implementation (Fig. 5.)

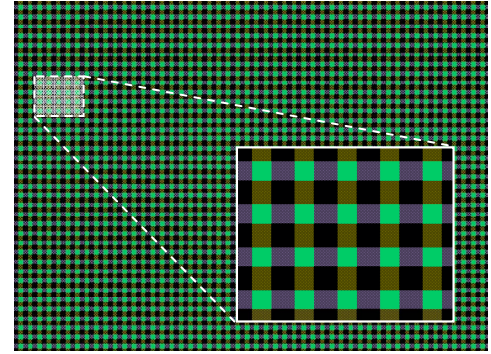


Fig. 5. The layout of PCMS array. The cross point array does not require additional strapping to reduce wordline or bitline resistance. The strapless cross point topology provides an ideal scaling path for $4\lambda^2$ implementation. CMOS circuit is placed under the memory array. High area efficiency is thus achieved.

To electrically access a bit in a memory block, V_{access} is applied to the selected column and 0V to the selected row. The deselected row and column biases must be chosen so that the voltage across each of the unselected cells is less than the minimum threshold voltage in the block, $\min(V_{t_{set}})$. This operating scheme can be modeled with an inhibiting factor, β , where $\beta = \min(V_{t_{set}}) / V_{access}$.

A. READ:

To ascertain the PCM state, a READ access bias is applied to the selected cell to threshold switch SET but not RESET. This access bias must be higher than the highest SET threshold voltage, $\max(V_{t_{set}})$. Therefore, the READ inhibiting factor is $\beta_R = \min(V_{t_{set}}) / \max(V_{t_{set}})$. Since the SET threshold voltage is dominated by the OTS switching mechanism, the OTS threshold distribution influences the inhibiting latitude in READ.

B. WRITE:

To program a bit, a WRITE access bias is applied to the selected cell. The access bias must be higher than the highest RESET threshold voltage, $\max(V_{t_{rst}})$. Hence, the WRITE inhibiting factor is $\beta_W = \min(V_{t_{set}}) / \max(V_{t_{rst}})$. Consequently, the tradeoff between design latitude and technology selection can be derived. The normalized threshold voltage window between SET and RESET,

$\Delta V_{t_{norm}}$ represents memory switching dynamic range. As illustrated in Fig. 6, the inhibiting scheme stops working as $\Delta V_{t_{norm}}$ approaches 150% empirically. Moreover, a smaller $\Delta V_{t_{norm}}$ yields a larger inhibiting factor. Larger inhibiting factors provide wider design latitude for the random access of a cross point array.

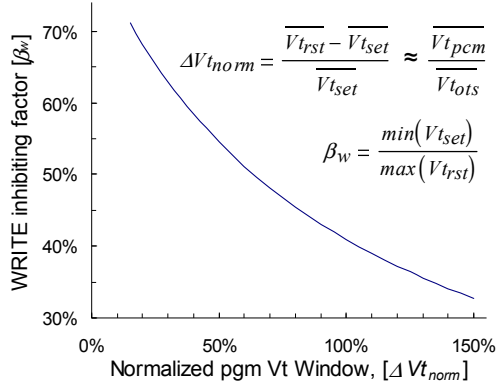


Fig. 6 Technology choice of device parameters vs. design latitude.

Experiments and Results

A. Physical construction:

A 64Mb PCMS cross point test chip is used as the technology vehicle in this research. Cell sizes ranging from 40nm to 230nm are explored. A 90nm CMOS technology provides the base process flow for PCMS integration. One memory layer is sandwiched between the 2nd and the 3rd levels of Cu interconnect (Fig. 7). The 3D SEM image illustrates the compatibility of PCMS with mainstream CMOS technology as well as the area efficient topology in the vertical stack.

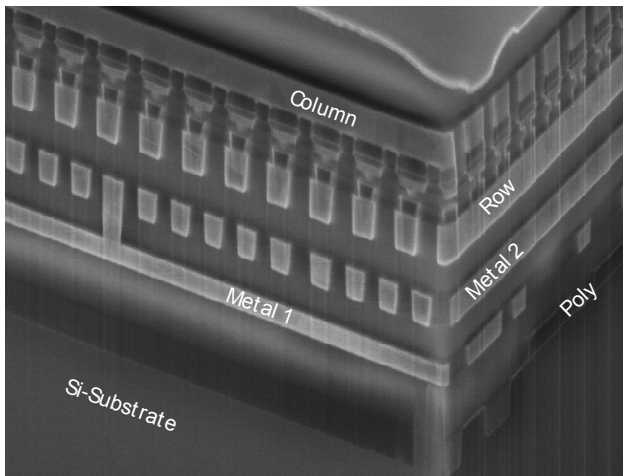


Fig. 7 One layer of the PCMS array fully integrated with a CMOS technology. The memory cell stack, including rows and columns, is shown sandwiched between M2 and M3. M3 is not shown.

B. Operations:

Fig. 8 exhibits the programming transfer characteristics of an array of 4096 independent, MOS-isolated bits. Each group of the box plot represents the intrinsic program distribution subject to each of pulse amplitudes.

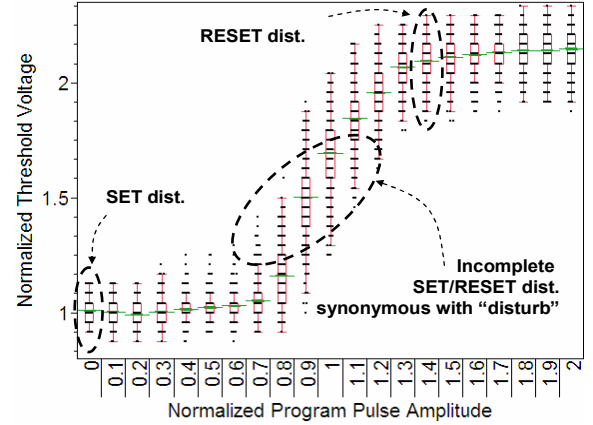


Fig. 8 Programming distribution of 4096 independent PCMS bits.

No cross point operating disturbance is expected since each of the bits in the array is MOS-isolated. However, operating disturbances in a true cross point array can occur and degrade distributions. For example, the program distribution can be modulated by adjusting inhibiting bias (Fig 9).

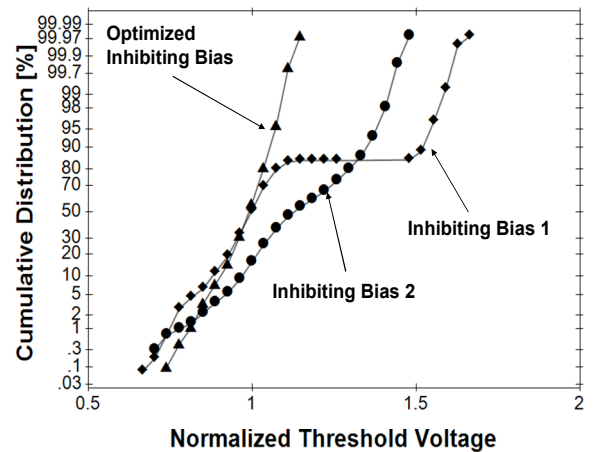


Fig. 9 WRITE disturbances can occur in a PCMS cross point array. The operating disturbance can be eliminated by bias optimization.

To eliminate the operating disturbance, inhibiting factor optimization, such as device threshold targeting and operating bias selection, must be deployed through proper balance between technology and design.

C. Performance:

In addition to PCM's non-volatility and cell-level alterability, PCMS is also capable of high bandwidth and

long endurance. For example, shown in Fig. 10, PCM's high speed vitrification capability (RESET operation) exhibits little or no degradation with OTS in series.

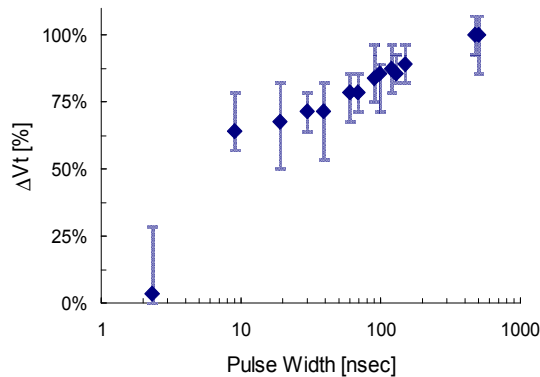


Fig. 10 PCMS is capable of high speed writes. Significant programmed Vt window is achieved at pulse width as narrow as 9 nanoseconds. The pulse amplitude is the same for all pulse widths.

Cycling endurance of 10^6 cycles is demonstrated (Fig. 11). More than 1 volt of dynamic range in a block of 2Mb makes PCMS a good candidate for high density parts (Fig. 12).

Conclusion

The Ovonic Threshold Switch enables area efficient memory layout and possesses compatible scaling attributes with PCM for future random access memory and solid state storage applications. Integrated with CMOS, PCMS provides the most promising NVM technology in scalability.

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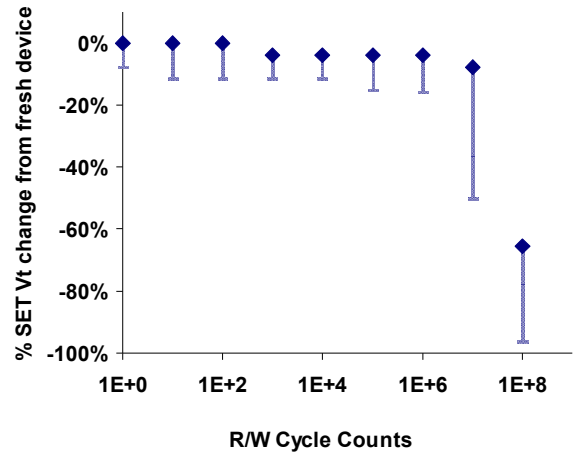


Fig. 11 PCMS cycling endurance: Cell SET Vt distribution vs. R/W cycling counts. Degradation tails (3.5σ) developed after 1 million cycles.

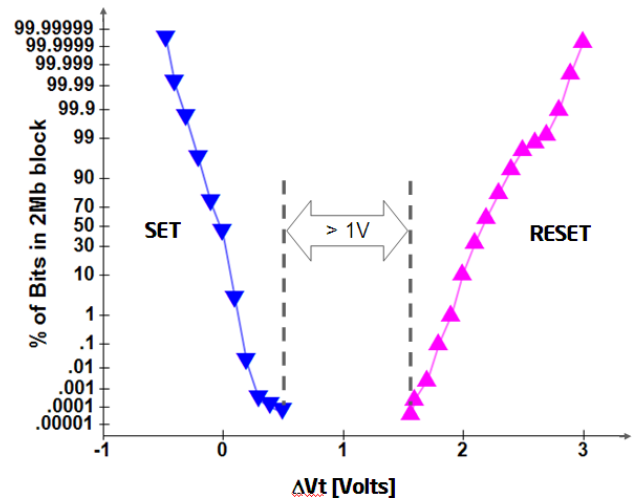


Fig. 12 RESET and SET distributions within a block of 2Mb. ΔV_t of x-axis is referenced to the mean V_t of SET state. This work demonstrates more than 1V of window in memory array.

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